Listing of Claims(clean version):

1. (Currently Amended) A circuit of a finite impulse response (FIR) filter comprises:
a transmission delay line configured to have at least one transmission line delay element with corresponding at least one delay-time;
an input signal coupled to an input of the transmission delay line; a termination impedance coupled to an output of the transmission delay line and configured to terminate the transmission delay line;
a first transconductance element coupled to the input signal and configured to multiply the input signal by a first filter coefficient and to convert the input signal to a first current;
at least one second transconductance element coupled to at least one corresponding output of the at least one transmission line delay element and configured to multiply at least one time-delayed input signal by at least one corresponding filter coefficient and to convert at least one multiplied time-delayed input signal to at least one second current;
an output of the first transconductance element and at least one second corresponding output of the at least one second transconductance element coupled together to form a current summing node for summing the first current and the at least one second current into a summed current;
a transimpedance element coupled to the current summing node and configured to convert the summed current to a filter output voltage signal.

2. (Currently Amended) The circuit of claim 1 wherein the input signal is single ended or differential and the output voltage signal is single ended or differential.

3. (Currently Amended) The circuit of claim 1 wherein the said transmission line delay elements configured as waveguides, microstrip lines, stripline transmission lines, coaxial lines or two-wire lines are implemented on an integrated circuit device, off an integrated circuit chip, on a semiconductor substrate, on a package substrate or on a printed circuit board (PCB).

4. (Currently Amended) The circuit of claim 1 wherein each of the said transmission line delay elements has a fixed or a programmable delay time.

5. (Currently Amended) The circuit of claim 1 wherein the transmission delay line comprises a fixed or programmable number of transmission line delay elements.

6. (Currently Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured as a transconductance amplifier, as a multistage voltage amplifier, resistors, or a combination of resistors and voltage amplifiers.

7. (Currently Amended) The circuit of claim 1 wherein each of the first transconductance element and the at least one second transconductance elements is configured to have a fixed value, a programmable value, or an adaptively controlled value.

8. (Cancelled)

9. (Currently Amended) The circuit of claim 1 wherein the termination impedance is configured to have a matched or mismatched impedance in response to a system filter requirement specification.

10. (Currently Amended) The circuit of claim 1 wherein the transimpedance element comprises a transimpedance amplifier configured for a fixed transimpedance, a programmable transimpedance, or an adaptively controlled transimpedance.

11. (Currently Amended) The circuit of claim 1 further comprises input matching impedance elements configured for matching to the corresponding inputs of the said transconductance elements.

12.-14. (Cancelled)

15. (Currently Amended) The circuit of claim 1 wherein the analog filter is configured as an finite impulse response (FIR) filter for equalizing an input signal in disk drives, optical , serial chip-to-chip, serial backplane high speed networks, or radio frequency communication systems.

16-30. (Cancelled)

Amendments to the Drawings:

The attached replacement sheets of drawings include changes to Figs 1, 2 and 4a and cancellation of Figs 3, 4b-14.

Attachments following last page of this Amendment:

Replacement Sheets (3 pages)